

REMARKS

Claims 2 and 10 have been amended, claims 4, 8, 9, 17 and non-elected claims 20 to 23 have previously been canceled, leaving claims 1 to 3, 5 to 7 and 10 to 19 active in this application.

Claim 1 was rejected under 35 U.S.C. 102(b) as being anticipated by Yamasaki et al. (U.S. 5,973,554). The rejection is respectfully traversed.

Claim 1 requires, among other features, a network of substantially coplanar power distribution lines laterally disposed on the first surface of the chip over the overcoat, located directly over active components of the circuit; the lines conductively connected to selected active components below the lines in a direction normal to the first surface through vias in the overcoat, the lines also connected by conductors to segments of the leadframe. No such structure is taught or suggested by Yamasaki et al. either alone or in the combination as claimed. A review of Yamasaki et al. will reveal that the structure therein is a single transistor having a single Vcc line and a single Vss line which are not coplanar and laterally disposed on the first surface. Furthermore, the claim requires active components in the plural which are not shown in Yamasaki et al. The power lines of the subject application, as claimed, power a plurality of active components, no such structure being shown or contemplated by Yamasaki et al.

Claims 2 to 5, 10, 12 to 16, 18 and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. in view of Tani (U.S. 5,468,993). The rejection is respectfully traversed.

Claim 2 includes the features discussed above with reference to claim 1, no such features being taught or suggested by Yamasaki et al. Tani fails to overcome the deficiencies noted above in Yamasaki et al. In this regard claim 2 requires, among other features, electrically conductive substantially coplanar, laterally disposed films deposited on the overcoat and patterned into a network of lines substantially vertically over the active components, the films in contact with the vias.

Claim 2 further requires at least one stress-absorbing film and an outermost film non-corrodible and metallurgically attachable. No such feature is taught or suggested either alone or in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claims 3 to 5, 10, 12 to 16, 18 and 19 depend from claim 2 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 2.

In addition, claim 3 further limits claim 2 by requiring that the chip be selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material customarily used in electrical device fabrication. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 5 further limits claim 2 by requiring that the integrated circuit comprise multi-layer metallization, at least one of the layers made of pure or alloyed copper, aluminum, nickel, or refractory metals. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 7 further limits claim 2 by requiring that the leadframe comprise a sheet-like material selected from a group consisting of copper, copper alloy, aluminum, iron-nickel alloy, or invar. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 10 further limits claim 2 by requiring that leadframe segments be shaped as leads solderable to outside parts. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 12 further limits claim 2 by requiring a wire bond to the electrical conductors connecting the network lines with the second plurality of segments. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 13 further limits claim 2 by requiring that the electrically conductive films comprise at least one stress-absorbing metal layer selected from a group consisting of copper, nickel, aluminum, tungsten, titanium molybdenum, chromium, and alloys thereof. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 14 further limits claim 2 by requiring that the outermost metal layer be selected from a group consisting of pure or alloyed gold, palladium, silver, platinum, and aluminum. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 16 further limits claim 15 by requiring that the bonding wire be selected from a group consisting of pure or alloyed gold, copper, and aluminum. No such feature is taught

or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 18 further limits claim 2 by requiring that the network of lines be electrically further connected to selected segments suitable for outside electrical contact. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claim 19 further limits claim 2 by requiring that the network of lines, together with the metal-filled vias, provide the power distribution function between the active circuit components. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani or any proper combination of these references.

Claims 6, 11 and 15 were rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki et al. in view of Tani in view of Wolf et al. publication. The rejection is respectfully traversed.

Claims 6, 11 and 15 depend from claim 2 and therefore define patentably over the applied references for at least the reasons presented above with reference to claim 2 since the Wolf publication fails to overcome the deficiencies in Yamasaki et al. as noted above.


Claim 6 further limits claim 2 by requiring that the overcoat comprise materials selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbon alloys, polyimide, and sandwiched films thereof. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani, Wolf publication or any proper combination of these references.

Claim 11 further limits claim 2 by requiring solder balls attached to the electrical conductors connecting the network lines with the second plurality of segments. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani, Wolf publication or any proper combination of these references.

Claim 15 further limits claim 2 by requiring that the conductors be bonding wires. No such feature is taught or suggested in the combination as claimed in either Yamasaki et al., Tani, Wolf publication or any proper combination of these references.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



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